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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,651	07/31/2003	Octavian Florescu	020556	3569

23696 7590 09/17/2004

Qualcomm Incorporated
Patents Department
5775 Morehouse Drive
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EXAMINER	
NGUYEN, LINH M	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,651	FLORESCU, OCTAVIAN	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-29 and 31-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9,10,16,20,25,26 and 32* is/are allowed.

6)☒ Claim(s) *1-4,6-8,11-15,17-19,21-24,27-29,31 and 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-4, 6-29 and 31-33 are presented in the instant application according to the Applicant's filing on 08/03/2004.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 13, 21 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Oosera et al. (JP. Patent No. JP409046189A).

With respect to claims 1 and 28, Oosera et al. discloses, in Figure 1, a clock distribution circuit ant a corresponding method comprising a) a clock source [10] to generate a clock signal [Ai]; b) a clock divider [11] to divide the clock signal and produce a divided clock signal, and including a flip-flop [D flip-flop] that introduces a clock-to-Q propagation delay to the divided clock signal; and c) a delay matching circuit [12] to distribute the clock signal, and to introduce a second propagation delay to the clock signal, the second propagation delay substantially matching the clock-to-Q propagation delay introduced in the divided clock signal by the flip-flop.

With respect to claim 3, Oosera et al. discloses, in Figure 1, that the delay matching circuit substantially mimics current sinking and current sourcing characteristics of the flip-flop.

With respect to claim 13, Oosera et al. discloses, in Figure 1, that clock divider includes a first asynchronous reset feature [CD of 11] and the delay matching circuit includes a second

asynchronous reset feature [CD of 12] that mimics operation of the first asynchronous reset feature.

With respect to claim 21, Oosera et al. discloses, in Figure 1, a) a signal source [10] to generate a signal, b) a signal distribution circuit [12] to modify the signal and distribute a modified signal, and including a flip-flop that introduces a clock-to-Q propagation delay in the modified signal; and b) a delay matching circuit [11] to distribute the signal and introduce a second propagation delay to the signal, the second propagation delay substantially matching the clock-to-Q propagation delay introduced in the modified signal by the flip-flop.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 4, 6, 7, 8, 11, 12, 14, 15, 17-19, 22-24, 27, 29, 31, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oosera et al. (JP. Patent No. JP409046189A) in view of Chen et al. (U.S. Patent No. 6,002,284).

With respect to claims 2, 4, 6, 12, 14, 18-19 and 29, Oosera et al. discloses, in Figure 1, a clock distribution circuit ant a corresponding method comprising a) a clock source [10] to generate a clock signal [Ai]; b) a clock divider [11] to divide the clock signal and produce a divided clock signal, and including a flip-flop [D flip-flop] that introduces a first propagation delay to the divided clock signal; and c) a delay matching circuit [12] to distribute the clock

signal, and to introduce a second propagation delay to the clock signal, the second propagation delay substantially matching the first propagation delay introduced in the divided clock signal by the flip-flop.

Oosera et al. lacks disclosing details of the delay matching including a multiplexer having a select line coupled to a clock source, transmission gates within the multiplexer to substantially mimic characteristics of a slave transmission gate in a flip-flop, inputs coupled to the multiplexer to substantially mimic characteristics of a master output driver of the flip-flop, and an output coupled to the multiplexer to substantially mimic characteristics of an output driver in the flip flop and the multiplexer includes a select line coupled to the clock source.

Chen et al. discloses, in Fig. 7, a delay matching including a multiplexer having a select line coupled to a clock source, transmission gates within the multiplexer to substantially mimic characteristics of a slave transmission gate in a flip-flop, inputs coupled to the multiplexer to substantially mimic characteristics of a master output driver of the flip-flop, and an output coupled to the multiplexer to substantially mimic characteristics of an output driver in the flip flop and the multiplexer includes a select line coupled to the clock source [CLK2,CLK2b].

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure the clock distribution circuit of Oosera with a delay matching in the form of a multiplexer to facilitate the required delay to enhance system synchronization since such circuit arrangement of the logic circuit for the stated purpose has been a well known practice as evidenced by the teachings of Chen et al.

With respect to claim 7-8, 11, 31 and 33, Oosera et al. discloses all of the claimed limitations as expressly recited in claims 1 and 28, except for the details of the delay matching including a multiplexer having a first input coupled to drive a first transmission gate, a second input coupled to drive a second transmission gate, a select input coupled to the clock source to selectively enable one of the transmission gates, and an output coupled to the first and second transmission gates, in which the transmission gates are configured to correspond substantially to a slave transmission gate in the flip-flop, the transmission gates are configured to correspond substantially in size to the slave transmission gate in the flip-flop, and an inverter coupled to the output of the multiplexer, wherein the inverter is configured to correspond substantially to an output driver in the flip flop.

Chen et al. discloses, in Fig. 7, a delay matching including a multiplexer having a first input [D] coupled to drive a first transmission gate [66,68,70,72], a second input [Db] coupled to drive a second transmission gate [74,76,78,80], a select input coupled to the clock source [CLK2, CLK2b] to selectively enable one of the transmission gates, and an output [input to 84] coupled to the first and second transmission gates, in which the transmission gates are configured to correspond substantially to a slave transmission gate in the flip-flop, the transmission gates are configured to correspond substantially in size to the slave transmission gate in the flip-flop, an inverter coupled to the output of the multiplexer, wherein the inverter is configured to correspond substantially to an output driver in the flip flop.

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure the clock distribution circuit of Oosera with a delay matching in the form of a multiplexer to facilitate the required delay to enhance system synchronization since such circuit

arrangement of the logic circuit for the stated purpose has been a well known practice as evidenced by the teachings of Chen et al.

With respect to claims 15, 17, 22-24 and 27, Oosera et al. discloses all of the claimed limitations as expressly recited in claims 14 and 21, except for the delay matching circuit includes a multiplexer having a select line coupled to a signal source; transmission gates within the multiplexer to substantially mimic characteristics of a slave transmission gate in a flip-flop; inputs coupled to the multiplexer to substantially mimic characteristics of a master output driver of the flip-flop; and an output coupled to the multiplexer to substantially mimic characteristics an output driver in the flip flop; a first input coupled to drive a first transmission gate, a second input coupled to drive a second transmission gate, a select input coupled to the signal source to selectively enable one of the transmission gates, and an output coupled to the first and second transmission gates, wherein the transmission gates are configured to correspond substantially to a slave transmission gate in the flip-flop; the transmission gates are configured to correspond substantially in size to the slave transmission gate in the flip-flop.

Chen et al. discloses, in Figure 7, a multiplexer having a select line coupled to a clock source [CLK2, CLK2b], transmission gates [(66,68,70,72); (74,76,78,80)] within the multiplexer to substantially mimic characteristics of a slave transmission gate in a flip-flop, inputs coupled to the multiplexer to substantially mimic characteristics of a master output driver of the flip-flop, and an output coupled to the multiplexer to substantially mimic characteristics of an output driver in the flip flop, a select line coupled to the clock source [CLK2,CLK2b], a first input [D] coupled to drive a first transmission gate [66,68,70,72], and a second input [Db] coupled to drive

a second transmission gate [74,76,78,80], the multiplexer further including a select input coupled to the clock source [CLK2,CLK2b] to selectively enable one of the transmission gates, wherein the output is coupled to the first and second transmission gates and the transmission gates are configured to correspond substantially to slave transmission gates in a flip-flop.

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure the clock distribution circuit of Oosera with a delay matching in the form of a multiplexer to facilitate the required delay to enhance system synchronization since such circuit arrangement of the logic circuit for the stated purpose has been a well known practice as evidenced by the teachings of Chen et al.

Allowable Subject Matter

5. Claims 9-10, 16, 20, 25-26 and 32 are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter.

The closest prior art on record does not show or fairly suggest a delay matching circuit including a PMOS transistor having a drain coupled to the first input, a gate coupled to ground, and a source coupled to a supply voltage, wherein the PMOS transistor is configured to correspond substantially to a PMOS transistor in a master output driver of the flip-flop; and b) an NMOS transistor having a drain coupled to the second input, a gate coupled to the supply voltage, and a source coupled to ground, wherein the NMOS transistor is configured to correspond substantially to an NMOS transistor in the master output driver of the flip-flop, as called for in claims 9, 16, 20 and 25.

Remarks

7. Applicant's arguments filed 08/03/2004 have been fully considered but they are not persuasive. Amendment to claims 14 and 21 necessitates new ground of rejection based on the combination of Oosera et al. and Chen et al..

With respect to the Applicant's argument on claims 1, 3, 5, 13, 28 and 30, at page 13, third paragraph, the examiner disagrees with the Applicant's statement of "Oesera et al. does not provide circuitry for introducing a propagation delay that substantially matches a clock-to-Q propagation delay of the flip-flop in clock divider 11. Instead, Oosera et al. describes a delay circuit 12 with a flip-flop that appears to match a reset-to-Q delay in flip-flop 11". As clearly shown a) in Figs. 1a-b of Oesera et al., delay circuit 12 shows a flip-flop that matches a clock-to-Q propagation of flip-flop 11 and b) in the abstract, lines 9-11, "the clock signal received from the clock signal source 10 is passed to circuit 12 with a signal delay equal to a signal delay of the frequency divider circuit". Contrary to the Applicant's analysis, flip-flop 12 does not match a reset-to-Q delay in flip-flop 11, in addition to being coupled to the clock input [CP] the clock source [10] also is coupled to the set/reset input [CD], not to match the clock-to-Q delay in the flip-flop driver 11, but rather to provide asserting and deasserting the output of the delay matching circuit 12. Moreover, Fig. 1b evidently shows the delay of signal Bo from the clock divider 11 equals the delay of signal Ao from the delay circuit 12. Thus, Oesera et al. does provide circuitry for introducing a propagation delay that substantially matches a clock-to-Q propagation delay of flip-flop in clock divider 11; hence, the Oosera et al. reference anticipates claims 1, 3, 13 and 28.

With respect to the Applicant's argument on claims 14, 15 and 17, at page 14, it is moot since the claims are currently rejected on a new ground necessitated by the amendment based on the combined teachings of Oosera et al. and Chen et al.. Regarding the argument of claim 21 on the same page, claim 21 was inadvertently included in the rejection of Chen et. al., it is currently included in the rejection of Oosera et al. See above paragraph for response to similar argument regarding claim 21.

With respect to the Applicant's argument on claims 2, 4, 6, 12 and 29, at page 16, fourth paragraph, the Applicant seems to particularly argues about claim 2, which is currently rejected based on a new ground of rejection with the combined teachings of Oosera et al. and Chen et. al., the rejection is necessitated by the amendment to claim 2.

With respect to the Applicant's argument on claims 4, 6, 12 and 29, at page 16, fifth and sixth paragraphs, the Applicant stated that " one of ordinary skill in the art would have found no reason to consult Chen et al. for modifications to the Oosera et al. circuit". The examiner disagrees with the Applicant. Since Oosera et al. circuit encompasses all the components claimed except for the detailed configuration of the delay circuit and Chen et al. discloses such configuration, it would have been obvious to combine the teachings of Oosera et al. and Chen et al. so that one skills in the art would obtain a circuit as claimed with the provided matching delay.

With respect to the Applicant's argument on claims 7, 8, 11, 31 and 33 on page 17 and 22-24 and 27 on page 16 bridging page 17, see response from the above paragraph since the argument on these claims addresses similar issue.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Fri, Monday - Thursday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER